DPLL Adaptation and *I*/*Q* Imbalance Compensation for Mobile Satellite Demodulators

S. Jayasimha, T. P. Kumar and P. Jyothendar

Signion Systems Ltd., Hyderabad, India
info@signion.com

Abstract

To address two important performance-limiting issues of low-cost mobile satellite hand-held terminals, oscillator phase noise and adjacent channel interference, we present a low-complexity digital phase lock loop bandwidth adaptation and a novel amplitude phase imbalance compensator (scheduled after frequency locking a demodulator, but prior to achieving symbol timing recovery and unambiguous phase lock).

Index Terms— Amplitude estimation, compensation, phase estimation, phase-locked loops, phase noise.

1. Introduction

Processing architectures of low cost satellite hand-held terminals, with small antenna aperture, are optimized to achieve interference suppression. For example, down-converters (from L- or S-band) may provide *Zero-IF* quadrature (*I*/*Q*) signals for ADC digitization and DSP demodulation/ decoding. Alternatively, a *Low-IF* architecture alleviates image rejection associated with flicker noise and signal independent d.c. offsets in quadrature paths. Fig. 1's S-band to low IF converter IC's output *I*/*Q* filters typically have wide (e.g., 17MHz) low-pass responses; thus, a tunable, higher quality factor input band-pass filter might limit input noise bandwidth (reducing required amplifier and ADC dynamic range in addition to total harmonic distortion and inter-modulation products at the *I*/*Q* converter's low-IF output).

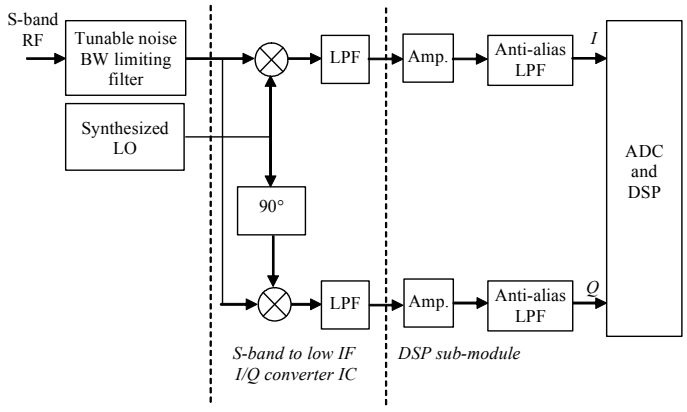

Figure 1: Low-cost low-IF Satellite Demodulator

Amplitude and phase imbalance of the quadrature paths result in image interference aliasing into the desired signal band, thus degrading receiver performance [1]. In addition, since optimum decision boundaries (as well as soft-decision computation) depend on *I*/*Q* amplitude and phase imbalance, as shown in Fig. 2 for BPSK, compensation is desirable.

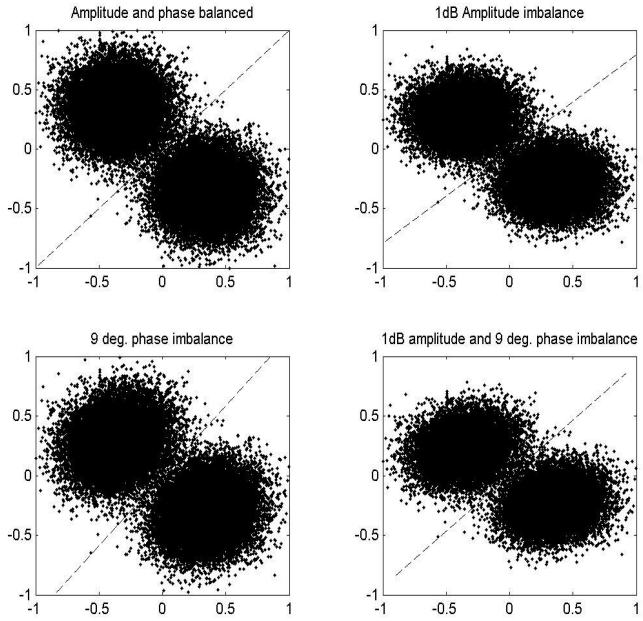

Figure 2: BPSK (in AWGN, E_b/N_0=9dB) decision boundaries

Though many techniques exist for *I*/*Q* phase and amplitude imbalance compensation in digital demodulators [2], they rely on extra hardware or firmware, to implement FFT or other such amplitude or phase estimation algorithm or adaptive noise canceller [3]. While other schemes to compensate imbalance, such as weighted amplitude and phase mean squared error minimization over the pass band [4], most modulation schemes have maximum power spectral density (PSD) at the carrier frequency. The calibration scheme presented separately minimizes amplitude and phase errors at the *operating* frequency, i.e. carrier frequency plus estimated offset (in a narrow band application, the offset, as a percentage of baud rate, can be significant). Further, our scheme exploits the frequency lock loop inherent to any digital demodulator, thereby minimizing additional logic required (by reusing existing firmware).

In addition, longer baud-rate duration signaling is more susceptible to phase noise (PN), which increases with carrier frequency (an ideal frequency multiplication by J increases the reference source's PN mask by $20\log J$, while an additional 2dB margin being allowed for practical realization [5]). For coded modulations, PN robust carrier synchronization techniques (with the complication that number of trellis states depending on oscillator PN) have been developed, e.g., a phase tracking Viterbi algorithm [6] and the Colavolpe-Barbieri-Caire (CBC) algorithm [7], which reduce

hand-held terminal cost by relaxing LO PN specifications. The PN distribution (assumed unimodal and symmetric in [6]) becomes biased (pg. 134 of [8]) in the presence of amplitude and/or phase imbalance (as in Fig. 2), substantially increasing error probability (unless phase states, for both algorithms, are discretized in a manner that accounts for the bias). Instead of these compute-intensive trellis augmentation schemes (which address the *strong* PN case), we describe a low-complexity adaptation of a decision-directed phase-lock loop (DDPLL) for a *moderate* PN oscillator. This case is of practical significance as recent manufacturing process advances have enabled inexpensive AT-cut crystal oscillators with tighter PN specifications. This method also extends to Costas loops (typically used where decisions cannot be made, e.g., interference cancellation for carrier-in-carrier communications [9]).

The overall scheme, described in the following sections, consists of four steps: a) DDPLL gain adaptation based on measured oscillator flicker and estimated thermal noise, b) amplitude imbalance estimation via variance measurements of quadrature paths after PLL stabilization, c) phase imbalance estimation based on already estimated amplitude imbalance and d) low pass filtered complex mixer outputs and compensation of both amplitude and phase imbalances.

Oscillator flicker and *I*/*Q* imbalance significantly degrade demodulator performance in the presence of in-band interferers (in particular, a negative frequency carrier at baseband), and the architecture and algorithms here are specifically designed for this scenario.

2. Digital PLL Gain Adaptation

PN defines the frequency domain uncertainty of an oscillator. Suppose an oscillator's output is $V(t)=V_0\cos[\omega_c t+\phi_c(t)]$, where $\phi_c(t)$ is random PN (in radians), i.e., $V(t)=V_0[\cos(\omega_c t)\cdot\cos\phi_c(t)-\sin(\omega_c t)\cdot\sin\phi_c(t)]$. Since $\phi_c(t)<<1$, $\cos(\phi_c(t))\approx 1$ and $\sin(\phi_c(t))\approx\phi_c(t)$, and $V(t)=V_0[\cos(\omega_c t)-\sin(\omega_c t)\cdot\phi_c(t)]$. In a PN measurement system, the oscillator's output, when multiplied with $\sin(\omega_c t)$ and low-pass filtered (to reject the double frequency term), yields $V(t)=0.5\cdot V_0[1-\phi_c(t)]$, and the SSB PSD of $\phi_c(t)$ relative to unity (the first term) is the PN spectral power of the oscillator in dBc/Hz.

A coherent demodulator's phase detector output, based on matched filtered in-phase (*I*) and quadrature (*Q*) components, i.e., $\tan^{-1}(Q/I)$, is periodically sampled, either every symbol, or once every *L* symbols (a block phase estimator [10]). The variance of the phase-detector's discrete-time phase estimate is the sum of all the synthesizers' PN and the PN induced by thermal noise. Discrete-time PN of the former may be modeled (using the method of [11]), from manufacturer–supplied synthesizer's PN plot, as shown by Fig. 3.

For example, the simulated phase spectrum of Fig. 4 represents the discrete-time PN spectrum (for a sampling rate, f_s, which for the purposes of performance evaluation is taken equal to the baud rate, here 9600Hz) of $\{\phi_c(k)\}$ of the, say, S-band carrier (at 2GHz) synthesized from a low-cost 10MHz AT-cut crystal oscillator (whose flicker psd is, similar to the typical PN density on pg. 88 of [8], approximately $f^{-1.5}$).

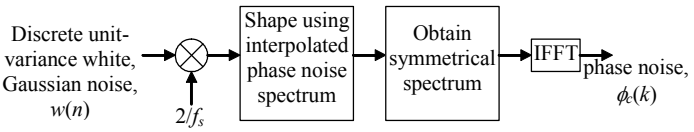

Figure 3: Discrete PN generation

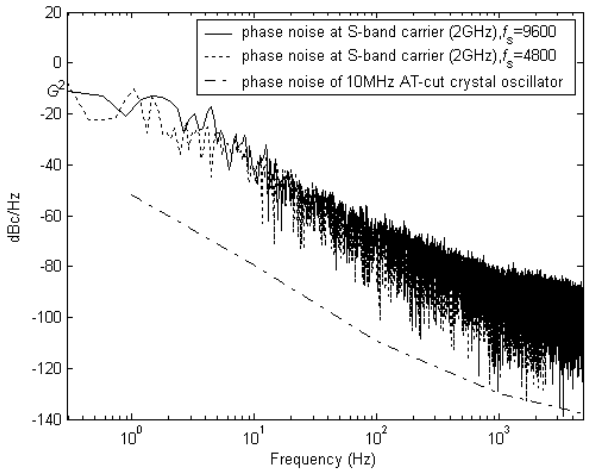

Figure 4: Discrete-time PN spectrum

When PN (not necessarily conforming, as in some literature, to a Wiener model) variance, $\sigma_{\Delta w}^2$, is significant when compared to noise variance, σ_n^2, the loop bandwidth of the decision-directed phase-lock loop (DDPLL) may be tuned (via a parameter *K*) as depicted in Fig. 5. Suppose the oscillator's PN low frequency PSD i.e., the power in the 0th bin of a discrete Fourier Transform (DFT) divided by the DFT's bandwidth as shown in Fig. 4, is G^2 and the oscillator's known PN bandwidth is *C* (which can be taken as 3-dB bandwidth of oscillator's PN; for Fig. 4's oscillator *C* is about 10Hz). Thus, the oscillator induced phase error variance, σ^2_{OSC}, is $(C\cdot f_s/N)\cdot(G/K)^2$, for a 1st order DDPLL, where the carrier phase estimate θ_n at the *n*th baud is updated from the carrier phase estimated at the previous baud according to $\theta_n=\theta_{n-1}+K\cdot\Delta\theta_n$ ($\Delta\theta_n$ being the *n*th baud's phase detector output) and $(C\cdot f_s/N)\cdot[G(1-K)/K]^2$, for a 2nd order DDPLL, where $\theta_n=\theta_{n-1}+K\cdot(\theta_{n-1}-\theta_{n-2})+K\cdot\Delta\theta_n$. The overall (observed) PN variance, $\sigma^2_{\Delta\hat{\theta}}$, is the sum of the oscillator induced PN variance, the phase error variance due to thermal noise i.e., $\pi B_L T_s/[4L\cdot(E_b/N_0)]$ for a DDPLL and $(N_0B_L/P^2)\cdot(P+N_0B_L)$ for a Costas loop (pg. 128 of [8]), where B_L is the phase detector's loop bandwidth, T_s is the symbol rate and *P* is the signal power, and the driving PN variance, $\sigma_{\Delta w}^2$. The estimated PN power for an *L*-baud block phase estimator, considering the loop-bandwidth of a 1st order DDPLL is therefore:

$$\sigma^2_{\Delta\hat{\theta}} = \left(C\cdot f_s/N\right)\cdot\left(G/K\right)^2 + \frac{K\cdot\left(1-K\right)^{-1/2}}{8L\cdot\left(E_b/N_0\right)} + \sigma^2_{\Delta w} \qquad (1)$$

where ($0<K<1$), and for a 2nd order DDPLL:

$$\sigma^2_{\Delta\hat{\theta}} = \left(C \cdot f_s / N\right) \cdot \left((1-K) \cdot G / K\right)^2 + \frac{K \cdot \left(1-3K\right)^{-1/2}}{8L \cdot \left(E_b / N_0\right)} + \sigma^2_{\Delta w} \quad (2)$$

where ($0<K<0.33$). Minimizing the two functions (1) and (2) with respect to K require K to be a root of a 8th order polynomial of the form x^8-$2x^6$+$4Ax^3$+$2x^2$-1 for 1st order DPLL and x^8-$2x^6$+$36Ax^5$+$72Ax^3$+$2x^2$-1 for 2nd order DPLL, where $A=8\cdot(f_s/N)\cdot G^2\cdot L\cdot(E_b/N_0)\cdot C$. $\sigma^2_{\Delta\hat{\theta}}$ is a unimodal function of K in (0, 1) and (0, 0.33) for 1st and 2nd order cases and therefore a golden section search [12] in these intervals may be used to find K. In practice, a 2nd order DDPLL (that tracks frequency offsets) is used, with K initially chosen for a wide B_L to obtain rapid phase and frequency lock; thereafter K is reduced to a value ($K_{initial}$) for low cycle-slip probability in the PN estimation interval, and the final K being determined as a single-parameter table look-up (as detailed below); this procedure allows automatic update of K on demodulator power-on, slow fading (e.g., rain), or oscillator aging.

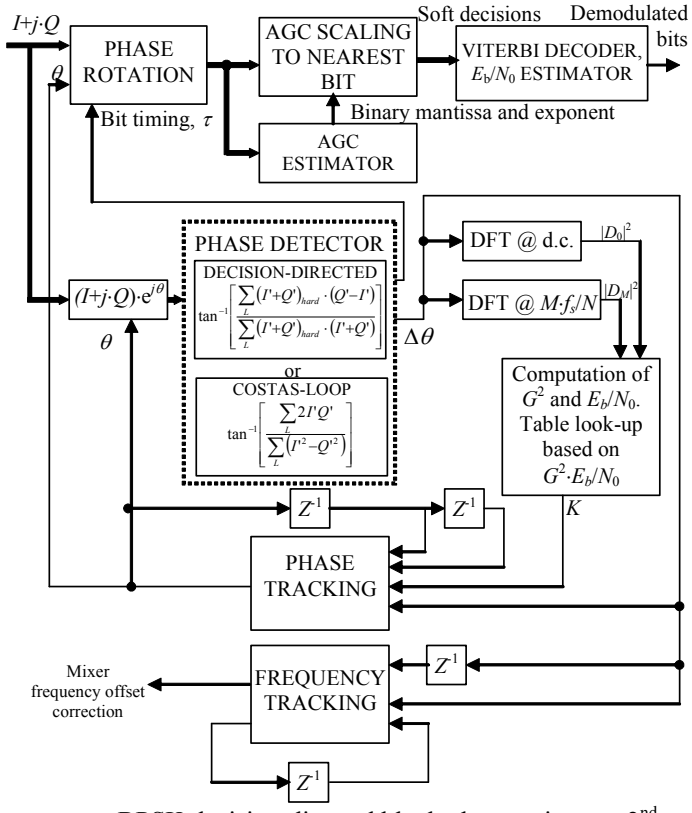

Figure 5: BPSK decision-directed block phase estimator, 2nd order phase tracker

Since oscillator flicker noise dominates the measured phase's low-frequency spectrum (from the output of the phase detector) G^2 is estimated from the power of an N-point DFT of phase detector outputs (in radians), $|D_0|^2$, of bandwidth f_s/N, centered at d.c. as $G^2=[(K_{initial})^2\cdot N\cdot|D_0|^2]/[C\cdot f_s\cdot(1-K_{initial})^2]$. A second N-point, bandwidth-f_s/N, DFT of phase detector outputs, $|D_M|^2$, (positioned at $M\cdot f_s/N$ where oscillator PN is negligible compared to independent of K thermal noise induced PN) obtains $E_b/N_0=f_s/(8L\cdot N\cdot|D_M|^2)$ for a 2nd order DDPLL. K is then obtained (see Fig. 6) via table look-up based on $G^2\cdot(E_b/N_0)=(K_{initial})^2/[8C\cdot L\cdot(1-K_{initial})^2]\cdot(|D_0|^2/|D_M|^2)$ (see Fig. 7). For low baud rate (i.e., low C/N_0), where PN is significant, a low-order phase modulation (i.e., BPSK) is preferred, where a thumb-rule (that increases carrier power by only a fraction of a dB of theoretical high-SNR AWGN performance) requires that the rms value of each baud's phase increment to be less than $\pi/10$ radians.

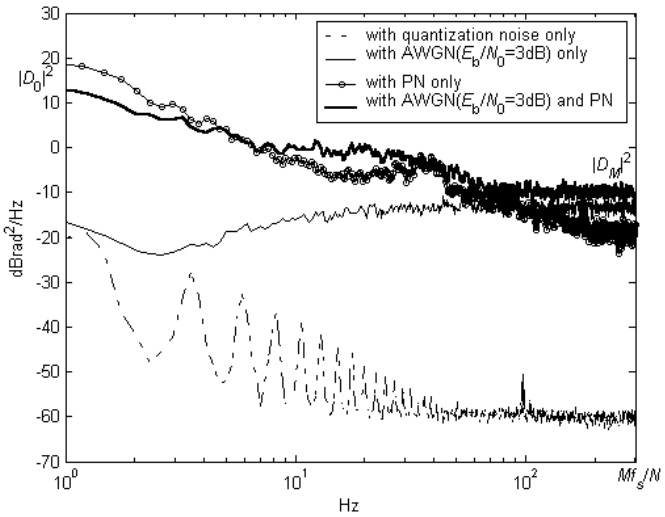

Figure 6: Decision-directed phase detector output's PSD for 4800bps BPSK with Fig. 4's oscillator PN, K=0.1 and M=N/2

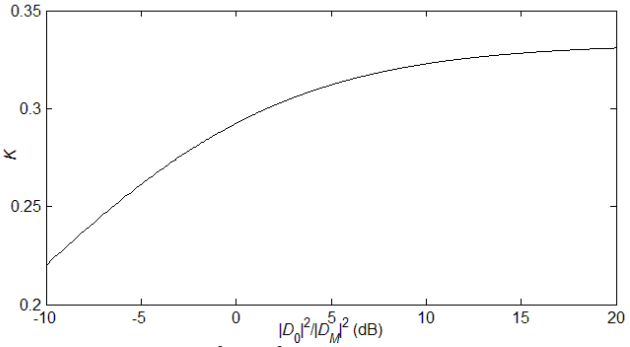

Figure 7: K vs. $|D_0|^2/|D_M|^2$, (C=10Hz, L=16, $K_{initial}$=0.1)

In addition to carrier induced PN, a decision-directed (narrowband) loop PN for BPSK, induced by decision errors due to noise alone is [8] $\sigma_\phi^2=(N_0B_L/P)/\{1\text{-}2Q[2(E_b/N_0)^{½}]\}^2$. The error probability, PE_ϕ, due to a phase error ϕ, the sum of phase errors induced by carrier PN and thermal noise is $PE_\phi=Q(2E_b/N_0)\cdot\cos\phi$. This error probability, averaged over the PN distribution, yields average BER. Fig. 8 shows that the E_b/N_0 for a given BER for BPSK, a constraint length 7, rate-½ coded, 4800 and 9600 baud rates with XO PN (of Fig. 4) degrades by only 0.4dB compared to when PN is absent. This also suggests a fixed DPLL gain, K, for a satellite link's PN specification and modulation/ coding scheme.

In burst-mode applications, K may be initialized based on nominal local oscillator PN and E_b/N_0, but subsequently calculated based on estimated PN (via carrier PSD computed on data-windows containing un-modulated carrier in each burst's preamble [13] on several bursts) and estimated E_b/N_0.

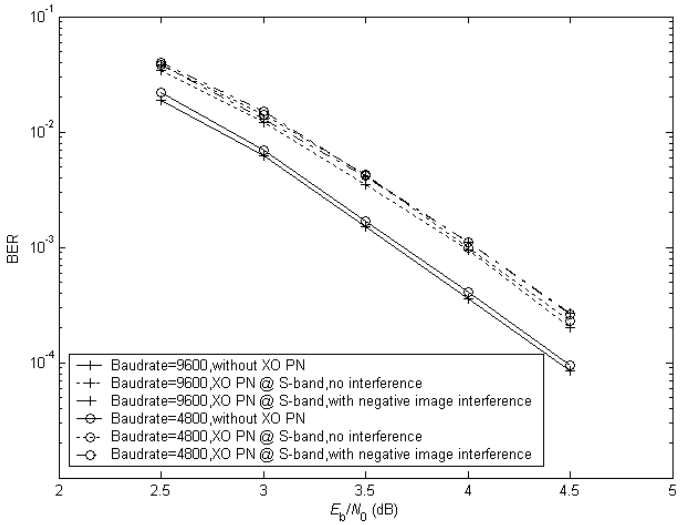

Figure 8: BER with DPLL gain adapted to K=0.33 (as compared to achieved performance with PN absent)

3. Amplitude Imbalance Estimation

Fig. 9 shows the flow of the amplitude and phase imbalanced quadrature signals through the input decimation filter, complex mixer and the low pass filter. Because I/Q calibration occurs after frequency lock, it has the advantage that it can be done through a transponder loop (thereby calibrating I/Q from the un-modulated received signal).

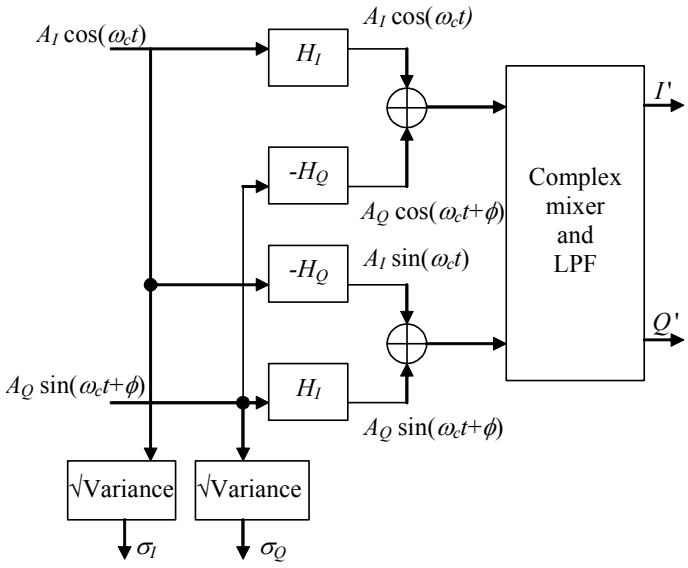

Figure 9: Uncompensated amplitude/ phase I/Q demodulator

Assuming that the analog signal processing chain's noise (contributed by amplifiers, filters and ADCs) of each quadrature path (up to where digital processing takes over) is proportional to the amplitude gain in that channel and that differential ADC quantization noise is negligible compared to signal amplitudes, the amplitude imbalance is obtained from *variance* estimates, σ_I^2 and σ_Q^2 (computed as the difference of mean-of-squares and square-of-mean, at the end of N sample block, during which summation of input samples and their squares are computed in parallel), of digitized samples of I and Q quadrature paths, with unmodulated carrier input, once the frequency PLL locks (without frequency PLL lock, a 50ppm clock can produce up to 2.5Hz offset at a 50kHz IF, or an unacceptable phase error of $2.5\times1024\times360/129600=7.1°$ in the N sample block) to the input. The number of samples, N, over which σ_I^2 and σ_Q^2 are measured is selected so that it is nearly a large M integer cycles, to minimize the estimation error. For the case of a 50kHz carrier and a sampling rate of 518400Hz, N may be selected around 1024 (to span about 100 carrier cycles) as:

$$N = rnd\left[rnd\left(\frac{1024 \times f_{NCO}}{f_s} \right) \cdot \frac{f_s}{f_{NCO}} \right] \tag{3}$$

f_{NCO} is NCO locked frequency and f_s the sampling frequency.

4. Phase Imbalance Estimation

After the amplitude imbalance estimation (and amplitude imbalance compensation using the result of the previous section), we compute r over N samples as, $r=(A_I^2+A_Q^2)^{1/2}$. Averaging both I' and Q' outputs of the complex mixer and LPF over N samples, the frequency, but not necessarily phase, locked, complex mixer's output shown in Fig. 9 is

$$\{[A_I\cos(\omega_c t)+A_Q\cos(\omega_c t+\phi)]+j[A_Q\sin(\omega_c t+\phi)+A_I\sin(\omega_c t)]\}e^{-j(\omega_c t+\theta)} \tag{4}$$

and can be written as

$$r\cdot e^{-j\theta}(\cos\psi+\sin\psi\cdot e^{j\phi}) \tag{5}$$

where $\sin\psi=A_Q/(A_I^2+A_Q^2)^{1/2}$, $\cos\psi=A_I/(A_I^2+A_Q^2)^{1/2}$ and $\psi=\tan^{-1}(A_Q/A_I)$. Approximating, for small ϕ, $\cos\phi\approx1-\phi^2/2$ and $\sin\phi\approx\phi$, (5) can be written as $I'+j\cdot Q'$, where

$$I' \approx r[\cos\theta(\cos\psi+\sin\psi-(\phi^2/2)\sin\psi)+\phi\sin\theta\sin\psi] \tag{6a}$$
$$Q' \approx r[-\sin\theta(\cos\psi+\sin\psi-(\phi^2/2)\sin\psi)+\phi\cos\theta\sin\psi] \tag{6b}$$

Let $\cos\psi=\cos(\xi+\pi/4)\approx 2^{-1/2}(1-\xi)$, $\sin\psi=\sin(\xi+\pi/4)\approx 2^{-1/2}(1+\xi)$. Thus, for small $\xi=\tan^{-1}(A_Q/A_I)-\pi/4$, $\cos\psi+\sin\psi=2^{1/2}$ and

$$I' \approx r\left[\cos\theta\cdot\left(\sqrt{2}-\frac{\phi^2}{2\sqrt{2}}(\xi+1)\right)+\frac{\phi\cdot(\xi+1)\cdot\sin\theta}{\sqrt{2}}\right]$$
$$Q' \approx r\left[-\sin\theta\cdot\left(\sqrt{2}-\frac{\phi^2}{2\sqrt{2}}(\xi+1)\right)+\frac{\phi\cdot(\xi+1)\cdot\cos\theta}{\sqrt{2}}\right] \tag{7}$$

Eliminating the unknown carrier phase θ,

$$I'^2+Q'^2 \approx r^2\left[2+\frac{\phi^4}{8}\cdot(\xi+1)^2-\phi^2\cdot(\xi+1)+\frac{\phi^2}{2}\cdot(\xi+1)\right]$$

$$\phi \approx \pm\sqrt{\left[\frac{2(1-\xi)}{(\xi+1)}-\frac{2\sqrt{2}}{(\xi+1)}\sqrt{\frac{(\xi-1)^2}{2}+\left(\frac{I'^2+Q'^2}{r^2}-2\right)}\right]} \tag{8}$$

Fig. 10 plots the amplitude-only $(I^2+Q'^2)/r^2$ discriminant function $(I'^2+Q'^2)/r^2$ with respect to phase imbalance. Since this measure has poor discrimination near zero phase, if estimated phase imbalance is assumed zero if the discriminant value is greater than 1.99869313, the maximum phase error magnitude is 0.0259 radians (or 1.48°). High (double) precision computations and high carrier C/N_0 are necessary to obtain ϕ with sufficient accuracy. The phase offset's sign is determined by trying both and applying the phase correction whose residual phase imbalance is close to 0.

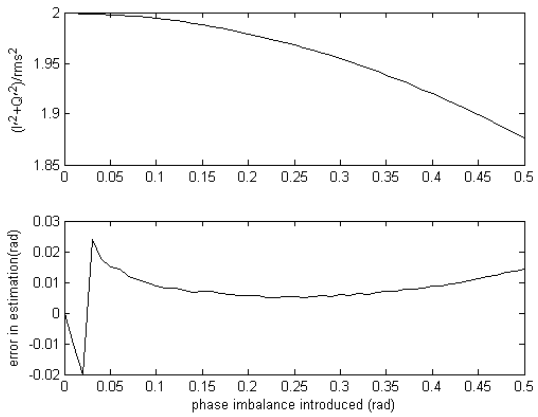

Figure 10: $(I^2+Q^2)/r^2$ discriminant (top) and phase estimate error (bottom) as functions of phase imbalance

5. Amplitude and Phase Imbalance Compensation

Amplitude imbalance is compensated by scaling each of the quadrature paths by the estimated input *rms* value of the other path, as shown in Fig. 11. Phase imbalance is compensated by subtracting ϕX from Q path:

$$X = A_I A_Q \cos(\omega_c t) \quad (9)$$

$$Y = \{A_I[A_Q \sin(\omega_c t \pm \phi)]\} \mp \phi X \quad (10)$$

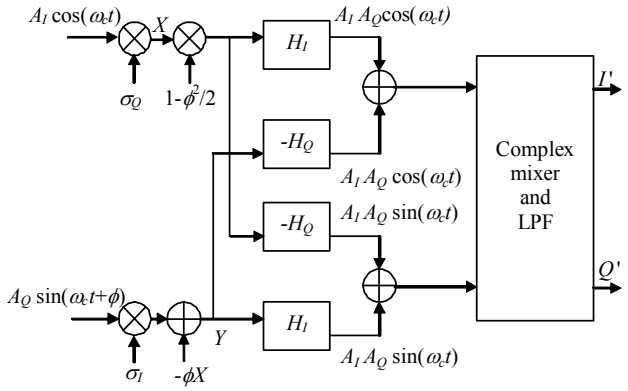

Figure 11: Amplitude and phase compensated I/Q demodulator

Fig. 12 shows E_b/N_0 vs. BER for 4800bps, constraint length 7, rate-½ coded, BPSK, without and with I/Q compensation.

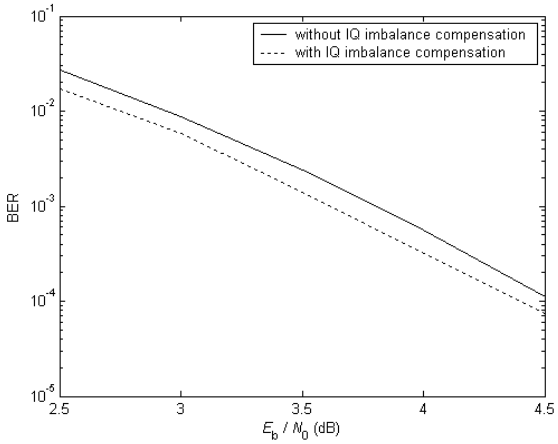

Figure 12: BER performance with -2dB amplitude and $\pi/8$ radians phase imbalance, before and after compensation

6. Conclusions

Low-cost mobile satellite terminals are being enabled by many single-stage S-band or L-band to baseband conversion ICs (some incorporating I/Q imbalance compensation for their analog outputs). Nevertheless, oscillator flicker, signal conditioning and ADC differential gain require digital compensation. We have described low-complexity algorithms that minimize performance degradation when oscillator PN and adjacent channel interference are present and shown their effectiveness.

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